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Agenda

- AMD Instinct™ Architecture
- AMD ROCm™ Software Stack
- OpenMP Offload Programming
- HIP and HIPifying Code
- Q&A
AMD Instinct™ Architecture
Industry’s First GPU to Break 10 TF (FP64) Barrier

2000 | ASCI White, #1 Supercomputer
     | 6 Megawatts, 212K Pounds (106 Tons), 12.3 Teraflops Peak

2020 | AMD Instinct™ MI100 GPU
     | 300 Watts, 2.56 Pounds (1.16 Kg), 11.5 Teraflops Peak
The Dawn of GPU-Accelerated Exascale: Major Leaps in Performance Driving Three Phases of Supercomputing

Performance of Top Supercomputers

- IBM ASCI White
- Cray Jaguar
- Titan
- Summit
- Frontier
- El Capitan

Application Optimized Architectures

HIGHEST EFFICIENCY THROUGH DOMAIN SPECIFIC OPTIMIZATION

- **AMD Instinct™ GPUs: Hardware and Software**

- **Application Optimized Architectures**

- **RDNA**
  - GAMING-OPTIMIZED GPU ARCHITECTURE

- **CDNA**
  - COMPUTE-OPTIMIZED GPU ARCHITECTURE

- EFFICIENCY

- REAL-TIME PIXEL RENDERING WORKLOADS
- COMPUTE INTENSE WORKLOADS

CHART FOR ILLUSTRATIVE PURPOSES
Data Center GPU Architecture Roadmap

- **2019**
  - **GCN**
    - First 7nm Data Center GPU
    - AMD Radeon Instinct™ MI50
  - **CDNA**
    - 2nd Gen AMD Infinity Architecture Optimized for ML/HPC
    - AMD Instinct™ MI100

- **2022**
  - **Advanced Node**
    - 3rd Gen AMD Infinity Architecture Extends to Exascale
    - "MINEXT" coming by year end 2021

Roadmaps Subject to Change
Node-level Design – GPU Hives

- GPUs can form “hives” of four GPUs
- One hives associated to one processor
- High-speed AMD Infinity Fabric™ connections in the hives (fully connected).
AMD CDNA™ Architecture – Made for Performance

- GPU is composed from several main blocks using an on-die fabric
- 120 Compute Units (CU)
  - Four Compute Engines w/ SIMD
  - SIMD pipelines execute 16-wide instructions
- Support for int8, FP16, FP32, FP64, bfloat16
AMD ROCm™ Software Stack
# Evolution of the AMD ROCm™ Software Stack

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<th>Applications</th>
<th>HPC Apps</th>
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**Processors**

CPU + GPU
Hands on Training Material at ROCm™ Learning Center

**ROCM™ Learning Center**

When it comes to solving the world’s most profound computational challenges, scientists and researchers need the most powerful and accessible tools at their fingertips. With the ROCm™ open software platform built for GPU computing, HIP and ML developers can now gain access to an army of different open compute languages, compilers, libraries, and tools that are both open and portable.

ROCM™ Learning Center offers resources to developers looking to tap the power of accelerated computing. No matter where you are in your journey, from those just getting started to experts in GPU programming, a broad range of technical resources below are designed to meet developers where they are at.

**Getting Started**

This module offers an introduction and sets you up for success with using ROCm™. The tutorials provide an overview of what ROCm is, and how to install the software to get started.

- **Introduction to ROCm™**
  - Watch Video
  - Download Presentation

- **ROCM™ Installation**
  - Watch Video
  - Download Presentation

**Fundamentals of HIP Programming**

This module provides in-depth training on programming with HIP. HIP is a high performance, CUDA-like programming model that is built on an open and portable framework. You will learn everything ranging from the basics of GPU programming to profiling GPU applications to an in-depth knowledge of programming with HIP.

- **Introduction to HIP**
  - Watch Video
  - Download Presentation

- **Deep Dive into GPU and Performance Optimizations**
  - Watch Video
  - Download Presentation

- **Your First HIP Code: Vector Add**
  - Watch Video
  - Download Presentation

**Deep Learning on ROCm**

This module includes hands on training for Deep Learning and equips you with the necessary knowledge on optimal usage of ROCm™ based systems.

- **Introduction to Deep Learning on ROCm**
  - Watch Video
  - Download Presentation

- **Running TensorFlow for MNIST Example**
  - Lab: TensorFlow & MNIST
    - Watch Video
    - Download Lab

- **Running PyTorch & LSTM Example**
  - Lab: PyTorch & LSTM
    - Watch Video
    - Download Lab

- **Multi-GPU Deep Learning**
  - Lab: Multi-GPU Deep Learning
    - Watch Video
    - Download Lab

- **Wrap-up: Deep Learning on ROCm**
  - Watch Video
  - Download Presentation

[Hands on Training Material at ROCm™ Learning Center](https://developer.amd.com/resources/rocm-resources/rocm-learning-center/)
### AMD Math Libraries for GPU (1/2)

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<th>Library</th>
<th>Description</th>
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<td>rocBLAS</td>
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</tr>
<tr>
<td>rocFFT</td>
<td>Fast Fourier Transforms</td>
</tr>
<tr>
<td>rocRAND</td>
<td>Random Number Generation</td>
</tr>
<tr>
<td>rocTHRUST</td>
<td>C++ Parallel Algorithms</td>
</tr>
<tr>
<td>rocPRIM</td>
<td>Optimized Parallel Primitives</td>
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</tbody>
</table>
AMD Math Libraries for GPU (2/2)

- **rocSPARSE**: Sparse BLAS, SpMV, etc.
- **rocSOLVER**: LAPACK Routines
- **rocALUTION**: Solvers and preconditioners for sparse linear systems

See [github.com/ROCm-Developer-Tools/HIP → hip_porting_guide.md](https://github.com/ROCm-Developer-Tools/HIP → hip_porting_guide.md) for a complete list.
Example: Calling BLAS Level 3 Routines (SGEMM)

Calling standard math library (host):

```c
void example_sgemm_host() {
    // Declarations omitted.

cblas_sgemm(transa, transb,
    m, n, k,
    alpha, A, lda,
    B, ldb,
    beta, C, ldc);
}
```

Calling rocBLAS math library (GPU):

```c
void example_sgemm_gpu() {
    // Declarations omitted.
    // Assume matrix on GPU.
    rocblas_handle handle;
    rocblas_create_handle(&handle);
    rocblas_sgemm(handle,
    transa, transb,
    m, n, k,
    &alpha, A, lda,
    B, ldb,
    &beta, C, ldc);
    rocblas_destroy_handle(handle);
}
```

Library interface almost identical and easy to port from host usage to GPU usage.
OpenMP Productive Programming for GPUs
Example: saxpy() – Very Common Operation in HPC Codes

```c
void saxpy(size_t n, float a,
           float * x, float * y) {
    double t = 0.0;
    double tb, te;
    tb = omp_get_wtime();
    #pragma omp parallel for firstprivate(a)
    for (int i = 0; i < n; i++) {
        y[i] = a * x[i] + y[i];
    }
    te = omp_get_wtime();
    t = te - tb;
    printf("Time of kernel: %lf\n", t);
}
```

Timing code (not needed, just to have a bit more code to show 😊)

This is the code we want to execute on a target device (i.e., GPU)

Timing code (not needed, just to have a bit more code to show 😊)

Don’t do this at home! Use a math library for this!

c clang -fopenmp <other compiler flags> -o saxpy.o -c saxpy.c

Copyright OpenMP ARB, used with permission
OpenMP: Heterogenous Programming (aka Offloading)

- As of version 4.0, the OpenMP API supports offloading computation to GPUs.
- Similar device model compared to other heterogenous programming models:
  - One host for “traditional” multi-threading.
  - Multiple GPUs of the same kind for offloading.
  - GPU devices are accessible though a device ID (from 0 to \(n-1\) for \(n\) devices).

```c
!$omp target &
!$omp   map(aloc:A) &
!$omp   map(to:A) &
!$omp   map(from:A) &
call compute(A)
!$omp end target
```

Host memory

```
0xabc0
01010010011101
01001111010111
01111010111101
01001011100100
00101101001101
01001000110101
01000100010010
01001000110101
01000100010010
01000001000100
```

Device mem.
Example: saxpy() on a GPU

```c
void saxpy(size_t n, float a, 
           float * x, float * y) {
    double t = 0.0;
    double tb, te;
    tb = omp_get_wtime();
    #pragma omp target \ 
        teams distribute parallel for \ 
        map(to:x[0:SZ]) map(tofrom:y[0:SZ])
    for (int i = 0; i < SZ; i++) {
        y[i] = a * x[i] + y[i];
    }
    te = omp_get_wtime();
    t = te - tb;
    printf("Time of kernel: %lf\n", t);
}
```

- No need for boilerplate code to
  - allocate memory,
  - transfer data, and
  - synchronize GPU execution.
- Tightly integrates with multi-threaded execution on the host
- Directive-based language
  - Fortran!
  - (No need to switch to a different base language.)
- Descriptive and prescriptive model

```
c clang -fopenmp --offload-arch=gfx908 <other compiler flags> -o saxpy.o -c saxpy.c
```
HIP Programming and HIPifying Code
What is HIP?

AMD **Heterogeneous-compute Interface for Portability**, or HIP, is a C++ runtime API and kernel language that allows developers to create portable applications that can run on AMD’s accelerators as well as CUDA devices.

**HIP:**
- Is open-source!
- Provides an API for an application to leverage GPU acceleration for the hardware of your choice.
- Syntactically similar to the CUDA® API enabling developers familiar with CUDA programming to easily extend their knowledge to new hardware platforms.
- Most CUDA API calls can be converted in place.
- Supports a strong subset of CUDA runtime functionality and enables creative developers to innovate on multiple hardware platforms.
A Tale of Host and Device

Source code in HIP has two flavors: Host code and Device code

- The host is the CPU.
- Host code runs here.
- Usual C++ syntax and features.
- Entry point is the ‘main’ function.
- HIP API can be used to create device buffers, move between host and device, and launch device code.

- The device is the GPU.
- Device code runs here.
- Device codes are launched via “kernels”
- Instructions from the Host are enqueued into “streams”.
HIP API

- **Device Management:**
  - `hipSetDevice()`, `hipGetDevice()`, `hipGetDeviceProperties()`

- **Memory Management**
  - `hipMalloc()`, `hipMemcpy()`, `hipMemcpyAsync()`, `hipFree()`, `hipHostMalloc()`

- **Streams**
  - `hipStreamCreate()`, `hipSynchronize()`, `hipStreamSynchronize()`, `hipStreamFree()`

- **Events**
  - `hipEventCreate()`, `hipEventRecord()`, `hipStreamWaitEvent()`, `hipEventElapsedTime()`

- **Device Kernels**
  - `__global__`, `__device__`, `hipLaunchKernelGGL()`

- **Device code**
  - `threadIdx`, `blockIdx`, `blockDim`, `__shared__`
  - 200+ math functions covering entire CUDA math library.

- **Error handling**
  - `hipGetLastError()`, `hipGetErrorString()`
HIP Kernel for saxpy()

```c
__global__ void saxpy_kernel(size_t n, float a, float * x, float * y) {
    size_t i = threadIdx.x + blockIdx.x * blockDim.x;
    y[i] = a * x[i] + y[i];
}

void saxpy(size_t n, float a, float * x, float * y) {
    assert(n % 256 == 0);
    saxpy_kernel<<<n/256,256,0,NULL>>>(n, a, x, y);
}
```
AOMP Implementation Status

- Call HIP kernel with OpenMP-managed buffers \(\text{use\_device\_ptr}\) ✓

- Call OpenMP kernels with HIP-managed buffers \(\text{is\_device\_ptr}\) ✓

- HIP and OpenMP kernels co-existence in same translation unit ✗
Mixing OpenMP Offload and HIP Kernels

```c
__global__ void saxpy_kernel(size_t n, float a, float * x, float * y) {
    size_t i = threadIdx.x + blockIdx.x * blockDim.x;
    y[i] = a * x[i] + y[i];
}

void saxpy_hip(size_t n, float a, float * x, float * y) {
    assert(n % 256 == 0);
    saxpy_kernel<<<n/256,256,0,NULL>>>(n, a, x, y);
}

void example() {
    float a = 2.0;
    float * x = ...; // assume: x = 0xabcd
    float * y = ...;
    // allocate the device memory
    #pragma omp target data map(to:x[0:count]) map(tofrom:y[0:count])
    {
        compute_1(n, x); // mapping table: x:[0xabcd, 0xef12], x = 0xabcd
        compute_2(n, y);
        #pragma omp target update to(x[0:count]) to(y[0:count]) // update x and y on the target
        #pragma omp target data use_device_ptr(x,y)
        {
            saxpy_hip(n, a, x, y) // mapping table: x:[0xabcd, 0xef12], x = 0xef12
        }
    }
    compute_3(n, y);
}
```
Summary

- **AMD Instinct™ GPUs**
  - High-performance GPU architecture designed for HPC and AI/ML
  - >10TF FP64 performance

- **AMD ROCm™ Software**
  - Open-source!
  - Standards based: OpenMP
  - Portable: OpenMP, HIP
  - Easy to port: HIPification
Q&A

AMD Instinct
Endnotes

**MI100-05 – Slide 5**

Calculations performed by AMD Performance Labs as of Sep 18, 2020 for the AMD Instinct™ MI100 accelerator at 1,502 MHz peak boost engine clock resulted in 11.535 TFLOPS peak theoretical double precision (FP64) floating-point performance. The results calculated for Radeon Instinct™ MI50 GPU at 1,725 MHz peak engine clock resulted in 6.62 TFLOPS FP64. Server manufacturers may vary configuration offerings yielding different results. MI100-05

**MI100-14**

Testing Conducted by AMD performance labs as of October 30th, 2020, on three platforms and software versions typical for the launch dates of the Radeon Instinct MI25 (2018), MI50 (2019) and AMD Instinct MI100 GPU (2020) running the benchmark application Quicksilver. MI100 platform (2020): Gigabyte G482-Z51-00 system comprised of Dual Socket AMD EPYC™ 7702 64-Core Processor, AMD Instinct™ MI100 GPU, ROCm™ 3.10 driver, 512GB DDR4, RHEL 8.2 MI50 platform (2019): Supermicro® SYS-4029GP-TRT2 system comprised of Dual Socket Intel Xeon® Gold® 6132, Radeon Instinct™ MI50 GPU, ROCm 2.10 driver, 256 GB DDR4, SLES15SP1 MI25 platform (2018): Supermicro SYS-4028GR-TR2 system comprised of Dual Socket Intel Xeon CPU E5-2690, Radeon Instinct™ MI25 GPU, ROCm 2.0.89 driver, 246GB DDR4 system memory, Ubuntu 16.04.5 LTS. MI100-14

**MI100-15**

Testing Conducted by AMD performance labs as of October 30th, 2020, on three platforms and software versions typical for the launch dates of the Radeon Instinct MI25 (2018), MI50 (2019) and AMD Instinct MI100 GPU (2020) running the benchmark application TensorFlow ResNet 50 FP 16 batch size 128. MI100 platform (2020): Gigabyte G482-Z51-00 system comprised of Dual Socket AMD EPYC™ 7702 64-Core Processor, AMD Instinct™ MI100 GPU, ROCm™ 3.10 driver, 512GB DDR4, RHEL 8.2 MI50 platform (2019): Supermicro® SYS-4029GP-TRT2 system comprised of Dual Socket Intel Xeon® Gold® 6254, Radeon Instinct™ MI50 GPU, ROCm 3.0.6 driver, 338 GB DDR4, Ubuntu® 16.04.6 LTS MI25 platform (2018): a Supermicro SYS-4028GR-TR2 system comprised of Dual Socket Intel Xeon CPU E5-2690, Radeon Instinct™ MI25 GPU, ROCm 2.0.89 driver, 246GB DDR4 system memory, Ubuntu 16.04.5 LTS. MI100-15
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