Discussing First Results of the SPEC ACCEL OpenMP Suite with Target Directives

All the SPEC ACCEL Contributors

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Standards Performance Evaluation Corporation (SPEC)

• SPEC is a non-profit corporation formed to "establish, maintain and endorse a standardized set of relevant benchmarks that can be applied to the newest generation of high-performance computers"

• Composed of four groups
  • Graphics and Workstation Performance Group (GWPG)
  • High Performance Group (HPG)
  • Open Systems Group (OSG)
  • Research Group (RG)

• https://www.spec.org
The SPEC Consortium: Members and Associates

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SPEC High Performance Group (HPG)

- Develops benchmarks to represent high-performance computing applications for standardized, cross-platform performance evaluation.

- Benchmarks
  - SPEC OMP2012
  - SPEC MPI2007
  - SPEC ACCEL
SPEC Benchmark Philosophy

• The result of a SPEC benchmark is always a SPEC score.
  • Higher is better

• This score is always in relation to a reference machine.
  • Each benchmark has its own reference machine
  • For example, for SPEC ACCEL 1.2, the reference machine is:

    SGI C 3108-TY11 with accelerator NVIDIA Tesla c2070
SPEC Benchmark Philosophy cont’d

• SPEC (HPG) benchmarks are full applications.
  • Including all the overhead of a real application

• SPEC harness ensures correctness of results.
  • To detect “overly aggressive optimization”
  • To guard against tampering

• Each benchmark suite has a set of run rules.
SPEC Benchmark Philosophy cont’d

• Hierarchy within benchmark suits
  • Benchmark suite i.e. SPEC ACCEL
  • Benchmark i.e. OpenMP
  • Dataset size i.e. Medium
  • Component i.e. 550.md
SPEC Benchmark Philosophy cont’d

• Benchmarks support “Base” and “Peak” configuration
  • These yield separate SPEC scores.
  • “Peak” runs allow for more freedom.

• Base runs
  • The same compiler switches for all components
  • The same parallelism
  • Only portability switches allowed

  SPEC ACCEL 1.2 OMP uses some portability switches
SPEC Power

- SPEC provides a standard methodology to measure and report power usage which can be incorporated into a SPEC benchmark.

- Normalizes the power usage across the full run of the suite
Benchmark Development Process

• Group effort, with lots of discussions

• Final decisions are by vote, even though we strive for consensus

• Technical and managerial parts
  • Find benchmark components and define run rules

• Using SPEC provided tools
  • SVN, harness, “common rules”
  • Websites, mailing lists, meeting venues
• Provide a benchmark that target accelerators
• SPEC ACCEL 1.2 just got released: June, 2017
• Use different programming models: OpenCL 1.1, OpenACC 1.0 and OpenMP 4.5
• Portable across architectures (host, XeonPhi, GPUs, etc)
• A benchmark that works with at least two compilers
• Program one accelerator
• Helps evaluate performance portability of compilers and directives/languages

Active members in SPEC ACCEL:
- NVIDIA, SGI, Intel, IBM, AMD, Argonne, ORNL, HZDR, Oracle, University of Houston, University of Virginia, Aachen University, University of Illinois, Indiana University, TU-Dresden

*Present at the DOE workshop
OpenMP 4.5 – Performance Portability

Consensus and community discussion on how to write “performance portable” style in OpenMP 4+

- Initially members had different views
  - Experimented with different programming styles:
    - SIMD centric
    - Using nested parallelism
    - Using target combined directives with collapsed loops
  - Ported the benchmarks from OpenACC 1.0

- We agreed on some “guidelines” on how to write performance portable code
- We used these “guidelines” and successfully parallelized the 15 benchmarks with OpenMP 4.0
- While writing the benchmarks, OpenMP 4.5 came out
- We re-evaluated these “guidelines” to target OpenMP 4.5
- Tested different compilers, platforms, etc.
<table>
<thead>
<tr>
<th>OpenMP Benchmarks</th>
<th>Language</th>
<th>Origin</th>
<th>Domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.ostencil</td>
<td>C</td>
<td>Parboil, University of Illinois</td>
<td>Thermodynamics</td>
</tr>
<tr>
<td>504.olbm</td>
<td>C</td>
<td>Parboil, University of Illinois</td>
<td>CFDm Lattice Boltzmann</td>
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<tr>
<td>514.omriq</td>
<td>C</td>
<td>Rodinia, University of Virginia</td>
<td>Medicine</td>
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<tr>
<td>550.md</td>
<td>Fortran</td>
<td>Indiana University</td>
<td>Molecular Dyn.</td>
</tr>
<tr>
<td>551.palm</td>
<td>Fortran</td>
<td>Leibniz University of Hannover</td>
<td>Large-eddy sim.</td>
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<tr>
<td>552.ep</td>
<td>C</td>
<td>NAS Parallel Benchmarks (NPB)</td>
<td>Embarrassing P.</td>
</tr>
<tr>
<td>553.clvleaf</td>
<td>C, Fortran</td>
<td>Atomic Weapons Establishments</td>
<td>Hydrodynamics</td>
</tr>
<tr>
<td>554.cg</td>
<td>C</td>
<td>NPB</td>
<td>Conjugate Grad.</td>
</tr>
<tr>
<td>555.seismic</td>
<td>Fortran</td>
<td>GeoDynamics.org</td>
<td>Seismic Wave Modeling (PDE)</td>
</tr>
<tr>
<td>556.sp</td>
<td>Fortran</td>
<td>NPB</td>
<td>Scalar Peta-d solv</td>
</tr>
<tr>
<td>557.csp</td>
<td>C</td>
<td>NPB</td>
<td>Scalar Peta-d solv</td>
</tr>
<tr>
<td>559.miniGhost</td>
<td>C, Fortran</td>
<td>Sandia National Laboratory</td>
<td>Finite difference</td>
</tr>
<tr>
<td>560.ilbdc</td>
<td>Fortran</td>
<td>SPEC OMP2012</td>
<td>Fluid Mechanics</td>
</tr>
<tr>
<td>563.swim</td>
<td>Fortran</td>
<td>SPEC OMP2012</td>
<td>Weather</td>
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<tr>
<td>570.bt</td>
<td>C</td>
<td>NPB</td>
<td>BTS 3D PDE</td>
</tr>
</tbody>
</table>
Use OpenMP 4.5 “Accelerator Model”

Rely on compilers to generate implementation specific values for a given architecture:
- # of teams
- # thread_limit,
- # of threads – in parallel regions
- SIMD length
- dist_schedule – in distribute
- loop schedules – in parallel do

Compiler implementers should pick these values to enable performance portability. HPC compilers should generate platform specific optimizations.
OpenMP 4.5 “Performance Portable Style”

For level-1 parallel loop:
- #pragma target teams distribute parallel for simd

For perfectly nested parallel loops:
- Collapsed loops with the combined directive
  
  #pragma omp target teams distribute parallel for collapse(N)
  
  for(i=0;....)
  
  for(j=0;....)
  
  for(k=0;....)

For loop nests that we could not collapse:

- Parallelize the outer loops with teams distribute, parallel for
- Parallelize the inner loops always with SIMD

Using OpenMP 4.5 the user and programmer –

- We used combined directive and / collapse to specify the parallel potential on a given platform.
Experiences with OpenMP 4.5

Differences between OpenMP 4.0 and 4.5 that affected our porting:

**Reductions**
- In OpenMP 4.5 the default for scalars is `firstprivate` as a result reduction variables need to be mapped to/from
  ```
  #pragma omp target map(tofrom:sum)
  #pragma omp teams distribute parallel for reduction(+:sum)
  for(....) 
  sum = sum + ....
  ```

**Privatization**
- Avoid over-privatizing on multiple levels
- We should only privatize only at the parallelism level that is needed
  ```
  #pragma omp teams distribute parallel for  // private(yy, zz)
  for(i= .... )
  for(j= ... )
  #pragma omp simd private(yy,zz)
  for(z= ...
    yy =
    zz =
  ```
Only merge target regions when is safe to do so.

From:

```c
#pragma omp target teams distribute parallel for
  for(i=…)  
    c[i] =

#pragma omp target teams distribute parallel for
  for(i=…)  
    b[i] = a[i] + ….
```

To:

```c
#pragma omp target teams
#pragma omp distribute
  for(i=…)  
    c[i] =

#pragma omp distribute
  for(i=…)  
    b[i] = a[i] + ….  // if c were a, then we will have a race condition.
```
Implementation specific issues:

• Some compiler implementations may pick num_teams equal to one.
  • E.g. for some platforms: e.g. Xeon Phi, etc

• Other implementations may pick num_threads equal to one, when a parallel for is nested inside a teams distribute and when it contains “simd”

• Compiler implementations may have different strategies to implement “simd” on a given platform
  • Some compiler implementations may be ignoring “simd” or tuning on autovec

This makes debugging hard

• You need to test on multiple platforms to guarantee correctness
## OpenMP (16):

<table>
<thead>
<tr>
<th>Test Sponsor</th>
<th>System Name</th>
<th>Accelerator Name</th>
<th>Results</th>
<th>Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>HZDR</td>
<td>ASUS ESC4000 G3 Series</td>
<td>Intel Xeon CPU E5-2630 v3</td>
<td>1.97</td>
<td>Not Run -- --</td>
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<tr>
<td>Indiana University</td>
<td>Ninja Developer Platform Pedestal: Liquid Cooled</td>
<td>Xeon Phi 7210</td>
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<td>0.356 --</td>
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<td>Not Run 4.54</td>
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<td>Indiana University</td>
<td>HP Z820 Workstation</td>
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<td>Indiana University</td>
<td>Cray XC30</td>
<td>Intel Xeon E5-2697 v2</td>
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<td>Intel</td>
<td>Endeavour Node(Intel Xeon E5-2697 v4, 2.3GHz, DDR4-2400 MHz, SMT ON, Turbo OFF)</td>
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<td>3.56 -- --</td>
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<td>3.76 -- --</td>
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<td>Endeavour Node(Intel Xeon Phi CPU 7250F, 1.40 GHz, SMT ON, Turbo ON, flat MCDRAM)</td>
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<td>7.55 -- --</td>
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<td>Intel</td>
<td>Intel Server System R2208WFZS (2 x Intel Xeon Gold 6148, 2.40 GHz, SMT ON, Turbo ON) Endeavour Node</td>
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<td>Technische Universitaet Dresden</td>
<td>Intel Server System LADM000AP Family (Xeon Phi 7210, 1.3 GHz, 64 cores, 4 threads)</td>
<td>Intel Xeon Phi 7210</td>
<td>4.39</td>
<td>6.08 -- --</td>
</tr>
</tbody>
</table>

Last update: Wednesday, 6 September 2017, 18:07
Example of a published result:

**Hardware**

- **CPU Name**: Intel Xeon Phi 7210
- **CPU**: Intel Turbo Boost 2 Technology up to 1.50 GHz
- **CPU MHz**: 1300
- **CPU Max**: 1500
- **FPUs**: None
- **CPU(s) enabled**: 64 cores, 1 chip, 64 cores/chip, 4 threads/core
- **CPU(s) Orderable**: 1 chip
- **Primary Cache**: 32 KB L1 + 32 KB D on chip per core
- **Secondary Cache**: 1 MB L2 on chip per 2 cores
- **L3 Cache**: 16 GB L3 on chip per chip
- **Other Cache**: None
- **Memory**: 96 GB (6 x 16 GB 2Rx4 PC4-2400T-R, running at 1066 MHz)
- **Disk Subsystem**: 275 GB INTEL SSDSC2BB30
- **Other Hardware**: --

**Accelerator**

- **Name**: Xeon Phi 7210
- **Accelerator Vendor**: Intel
- **Type of Acceler**: CPU
- **Accelerator Connection**: N/A
- **Does Use**: Yes
- **ECC**:
- **Acceler**: Intel Xeon Phi 7210, SMT, ON, Turbo
- **Acceler Description**: ON
- **Cluster Mode**: On, Memory Mode: Cache
- **Acceler Driver**:

**Software**

- **Operating System**: CentOS Linux release 7.3
- **System**: 3.10.0-514.21.2.el7.x86_64
- **Compiler**: Intel Compiler C/C+/Fortran Version 17.0.1
  - 20161005
- **File System**: eXt4
- **System State**: Run level 3 (user-level)
- **Other Software**: FFTW 3.3.6/p11
Preliminary results are showing

• Benchmark is very new

• Only 16 reportable results (compared to 100s from other SPEC/HPG benchmarks)

• No official results yet for OpenMP 4.5 offload on GPUs
  • Major milestone may be hit by the end of the year where we will have reportable results
  • IBM OpenMP 4.5 compiler are still beta
  • Some vendors got access to the benchmarks recently (outside the HPG team) and are fixing compiler bugs.

• Compilers need optimize for each target architecture – unless they expect the user to auto-tune

• Compilers are still working on their OpenMP optimizations and few support multiple architectures.
  • e.g. We need OpenMP compiler that supports a variety of architectures: e.g. multicore, Xeon Phi and GPUs using target regions to do better performance portable studies.
Result Submission Process

- Obtain and install the benchmark
- Perform a valid run
- Supply hardware and software description
- Submit result for review (and publication) to SPEC HPG
  - 2 week review process
  - (Define embargo period)
- Use the result as you would like
SPEC MPI Accelerator Search Program

- Combine SPEC MPI and SPEC ACCEL benchmark suites into one.
  - Facilitate support for homogeneous and heterogeneous multi-node systems
  - MPI+X, where "X" is a node-level parallel programming model such as OpenACC, OpenMP, CUDA, OpenCL, Kokkos, TBB, etc.
  - Compute intensive

- Focus on hybrid programming with accelerators
  - Being able to run on a single nodes or up to N nodes.
  - Support one or M accelerators per MPI rank (multiple-accelerator programming)

- Represents the state of the art for the given field
  - Results needs to be validated numerically

- Submissions that are included in the benchmark suite will receive up to $5,000 and a licensed copy of the new benchmark suite when released.

- More information: [https://www.spec.org/hpg/search](https://www.spec.org/hpg/search)
Thank you!

Questions?